Remarks

Applicant submits this preliminary amendment in conjunction with the divisional application filed herewith. The present application is a divisional application of Serial No. 09/574,563 filed May 17, 2000.

Please charge any shortages of fees or credit any overcharges of fees to our Deposit Account No. 02-2666.

Respectfully submitted,
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VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

Page 1, paragraph starting on line 5, should be replaced with:

The present application is a divisional application of Serial No. 09/574,563, filed May 17, 2000, which is a divisional application of Serial No. 09/245,030, filed February 5, 1999, now U.S. Patent No. 6,207,994, which is a continuation-in-part application of Serial No. 08/744,182, filed November 5, 1996, now abandoned. This application is also related to Serial No. [_____] 09/245,029, filed [concurrently herewith] February 5, 1999, now U.S. Patent No. 6,168,983, and entitled, "Method of Making A High-Voltage Transistor With Multiple Lateral Conduction Layers". The related applications are assigned to the assignee of the present application.

Page 7, paragraph starting on line 20, should be replaced with:

Figure 1 illustrates an insulated-gate[,] field-effect transistor (IGFET) having a gate 12 (comprised, for example, of polysilicon), an insulating layer 20, comprised of silicon dioxide or another appropriate dielectric insulating material, and an underlying lightly-doped p-type substrate region 16. Gate 12, insulating layer 20 and substrate 16 together form the insulated gate region of the device. In one embodiment, the gate region is a metal-oxide semiconductor (MOS), and the IGFET is a MOS transistor.

Page 8, first paragraph, should be replaced with:

An optional p-type region 15 is disposed in substrate 16 spaced-apart from N-well region 17. Additionally, a p-type buried layer 35 may be included beneath P-well 15. A N+ source diffusion region 14 is shown formed in region 15. An IGFET channel region 28 is formed between N+ source

diffusion region 14 and N-well region 17. A source electrode 10 provides an electrical connection to N+ source diffusion region 14. Similarly, a drain electrode 11 connects to [a N +] N+ drain diffusion region 19. Source and drain electrodes 10 and 11 may comprise a number of widely used metals or metal alloys. Source electrode 10 is shown extending over an isolative layer 27 formed over gate 12 where it functions as a field plate.

Page 15, paragraph starting on line 23, should be replaced with:

With reference now to Figure 7, a top view of a HVFET 500 having inter-digitated source and drain "fingertip" regions is illustrated. Various cross-sectional side views of the device structure are shown in Figures 3, 8, 9 and 10. (Note that Figure 3 is a view taken along cut line A:A of Figure 7. Figures 1, 2, 4, 5, and 6 also show other possible cross-sectional views taken through line A:A.) Figure 7 shows HVFET 500 having a source fingertip 505 that includes a source electrode 10. Disposed on either side of source electrode [510] 10 are drain fingertips 515 and 520 included in drain electrode 11. Further disposed on either side of source electrode 10 are additional source electrodes 530 and 535. Gate 12, which may be constructed of polysilicon or other suitable materials, is located adjacent source electrode 10. Similarly, gates 545 and 550 are adjacent additional source electrodes 530 and 535.

Page 16, paragraph starting on line 18, should be replaced with:

With continued reference to Figures 7-10, field plate extensions 553 and 555 counteract voltage breakdown at drain fingertips 515 and 520. Field plate extensions 553 and 555 overlay and are separated from the polysilicon drain field plate 45 by an inter-level dielectric layer 50 [(see Figure 3)] (see

Figure 9). Note that along the sides of drain fingertips 515 and 520, drain field plate 11 has a substantially shorter extension beyond the polysilicon drain field plate 45 towards the source electrode 10. This is illustrated in, for example, in the previously described cross-section taken along cut line A:A in Figure 3.

Page 16, paragraph starting on line 26, should be replaced with:

Figure 9 is a cross-sectional side view taken along cut line C:C of Figure 8. Here, at drain fingertip 520, drain electrode 11 includes a drain field plate extension 555 to mollify the high electric field in this area. As can be seen, the drain electrode 11 has a portion that overlies the drain field plate 45 and extends laterally over the buried regions 60. In one implementation, field plate 555 extends laterally a distance (X) of approximately 20-80 microns past the end of drain field plate 45. This is a considerably larger extension than is found along line A:A of Figure 3, which may be, for example 10-20 microns. In this example the drain fingertip radii (defined from the axis of rotation to the farthest edge of drain diffusion region 19) may be 5 microns or less. Fabricating HVFET 500 with a small fingertip radius, of course, reduces the required silicon area for the transistor and thus lowers its cost.